

[0037 "Engineering/MIS Design"]

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A communications and storage products design engineer with 17 years' experience in managing, marketing, and developing high-performance I/O adapters, CPUs, networking and storage products for the world's largest computer manufacturer and leading computer peripheral companies.

A high-energy professional in search of a technical challenge that demands project organization skills, big-picture vision and a dedicated team leader.

EXPERIENCE

4 Ways Inc., Warwick, Rhode Island

2000-2007

Manager of Electrical Engineering

Directed a team of engineers and technicians designing and developing electronics for a 3-dimensional imaging equipment manufacturing company with annual sales of \$100 million.

- Created an electronics roadmap for the next two generations of products.
- Formalized, scheduled and completed first pass PCBs for five major next generation projects consisting of a main controller, a waveform generator, sensor and motion controllers, and a laser light loop detector.
- Reorganized the department's distribution of work based on talent and company goals. Recruited new electrical engineering staff. Created and implemented the department's \$900,000 budget.
- Modified engineering design practices that improved efficiency and design quality.
- Saved \$280,000 annually by replacing expensive components, using alternative suppliers and negotiating electronic supplier contracts.

Micro Electric Research, Providence, Rhode Island

1999-2000

Electrical Engineering Consultant

Constructed architecture and guided the implementation of higher performance and lower cost Gigabyte Ethernet and HiPPI I/O adapters. The HiPPI adapter permitted the company to satisfy a \$93 million government contract.

Texas Instruments, Indianapolis, Indiana

1990-1999

Advisory Engineer (1995-1999)

HACMP/6000 Market Development Department

Provided technical assistance to the marketing department and its clients concerning integration projects for the company's High Availability Cluster Multi-Processing (HACMP) software product, a program that provides software solution to prevent accidental application downtime. The department generated sales in excess of \$10 million. Projects involved high-speed channel connections, storage solutions, distributed storage management and fault tolerance issues.

- Provided technical product briefings to more than 80 prospective customers.
- Participated on the team that set marketing strategies for the product.

Communications and Storage Development Department

Architect and program manager for the High Performance Parallel Interface (HiPPI) Gigabyte I/O adapter. This adapter duplicated the performance of a \$130,000 Cray Supercomputer I/O Channel for a price of \$18,000. Adapter sales grew to more than \$3.6 million per year and facilitated more than \$150 million of additional systems sales. Participated in the architecture of the Fibre Channel Standard (FCS) Gigabyte I/O adapter. Wrote the firmware interface specification and directed its implementation.

Texas Instruments, Continued

- Designed the architecture for the hardware portion of the adapter and oversaw the detailed implementation.
- Authored and directed the software and hardware product testing plan. Worked with seven communications and storage vendors to insure product compatibility.
- Founded, with three other companies, the HiPPI Networking Forum (HNF) industry alliance. Participated in the Fibre Channel Standard Initiative (FCSI) industry group on profile development.
- Identified performance problems with TCP/IP and file system access codes, resulting in a 3,000% performance increase.

Staff Engineer (1993-1995)

RISC/6000 CPU Development

Participated in the development of the company's new RISC/6000 systems and CPUs. Established the CPU design and verification methodology for chip design.

- Led the debugging team for the RISC system CPU chip sets and reduced turnaround time by 80%.
- Led a multi-site team that tested and simulated the SJ0 CPU chip set, facilitating on-schedule delivery.

Senior Associate Engineer (1991-1993)

RISC/6000 Systems Architecture Department

Participated on a team that defined the future direction and architecture for the company's new engineering workstation products. This included the evaluation and selection of an I/O bus for each new product. Performed competitive analyses and defined the requirements for new products.

I/O VLSI Chip Logic Design

Contributed to the logic design of VSLI I/O channel chips for the Series/1 mid-range commercial server system. Designed and verified the logic for the memory management and performance monitor chips.

Associate Engineer (1991)

VLSI Circuit Design Department

Designed and coded an algorithmic Programmable Logic Array macro generator for the circuit design Series/1 processor. Designed VLSI circuit macros.

Engineering Co-op (1990)

VLSI Circuit Design Department

Designed and simulated a RAM macro and combinatorial logic circuits.

Sonar Development I Department

Designed and debugged new ALU plug-in modules for Sonar systems.

EDUCATION

Notre Dame University, South Bend, Indiana

Bachelor of Science, Electrical Engineering, Dean's List, GPA 5.93/6.00, 1989

Other: Business courses, Continuing Education and professional development courses

AWARDS

Outstanding Technical Achievement for an I/O Adapter Product
Division Award for RISC System/6000 CPU Development
Excellence Award for VLSI Design Tool Support